

AUS920000226US1

1/26

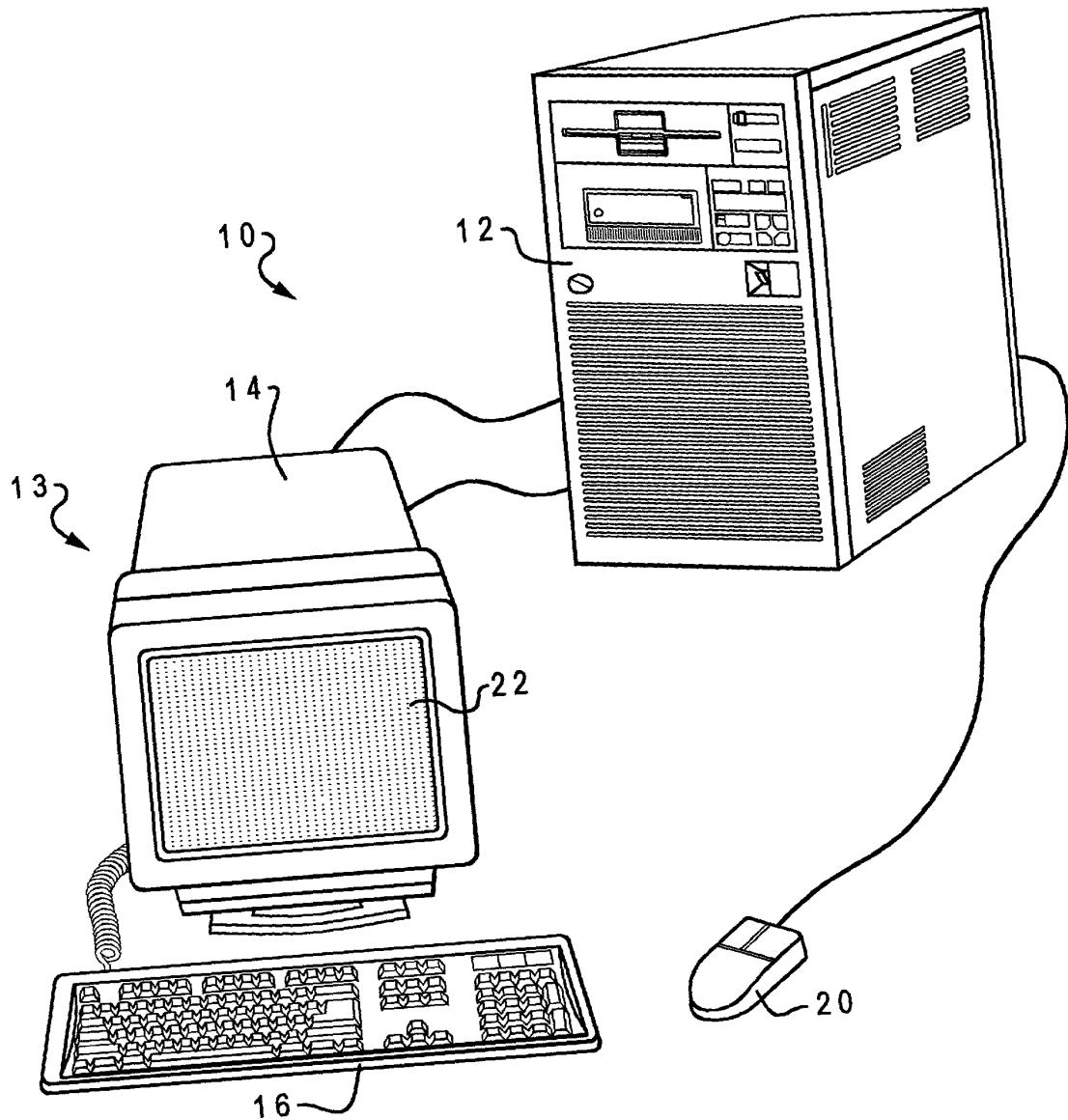
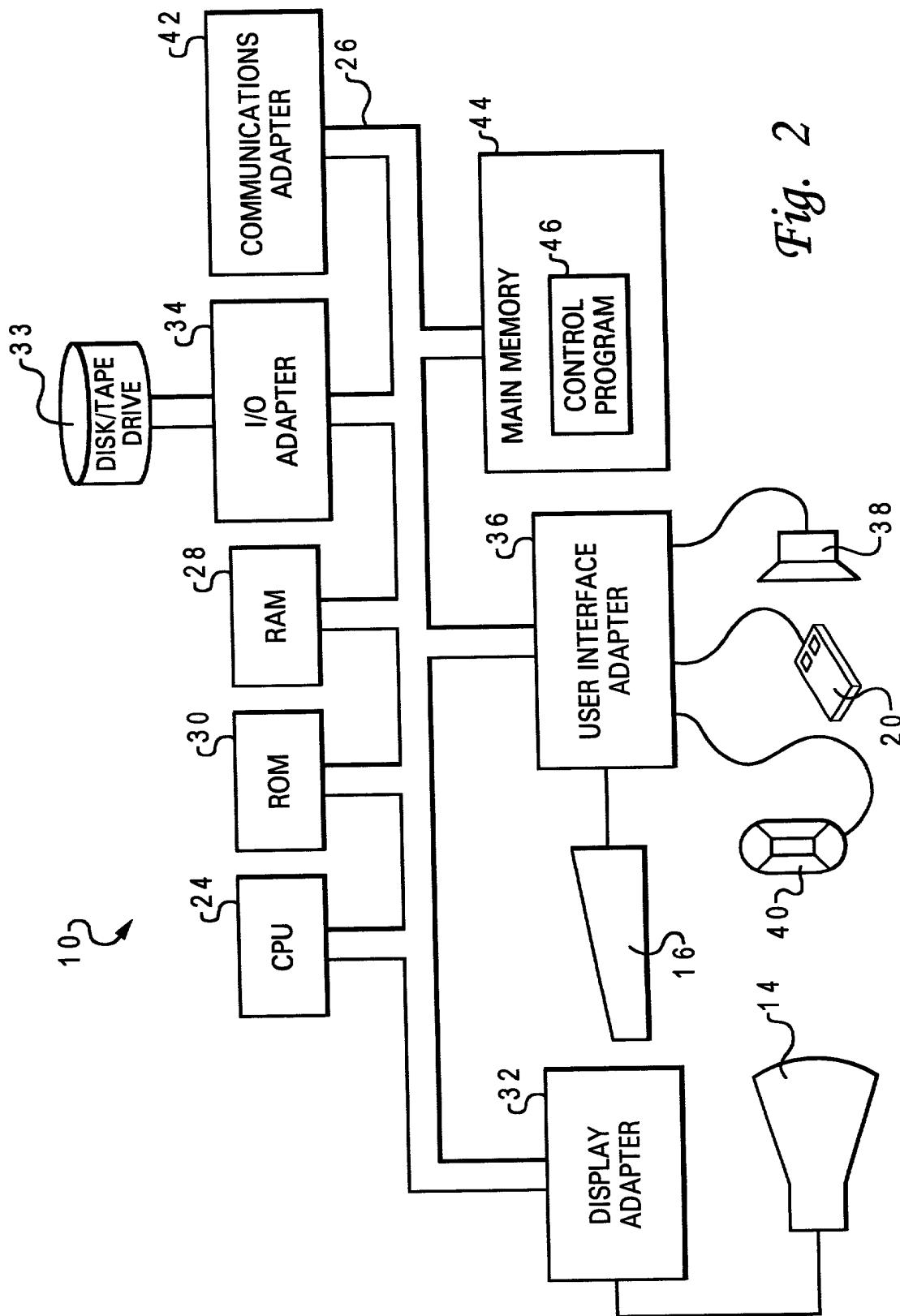


Fig. 1



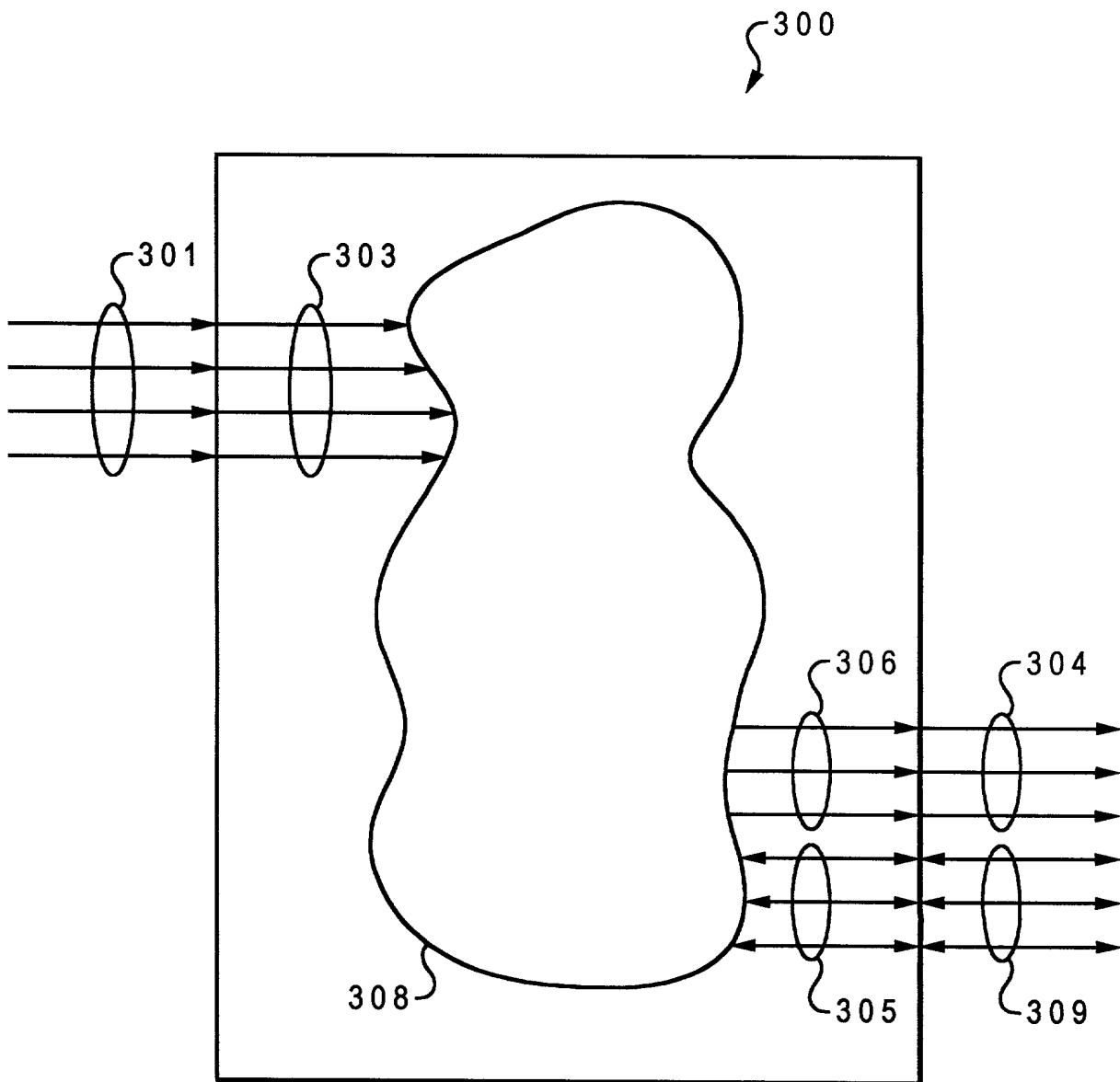


Fig. 3A

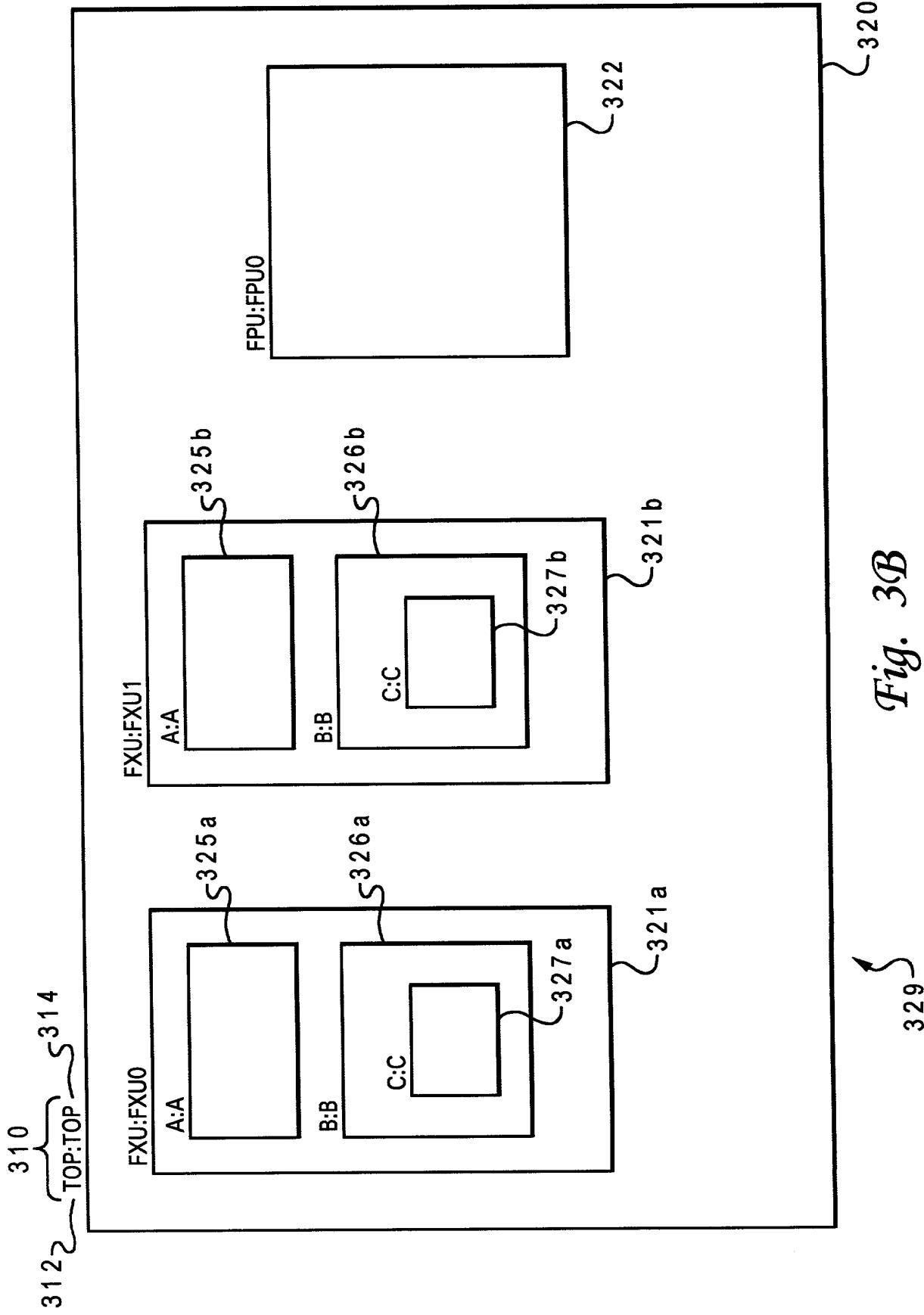


Fig. 3B

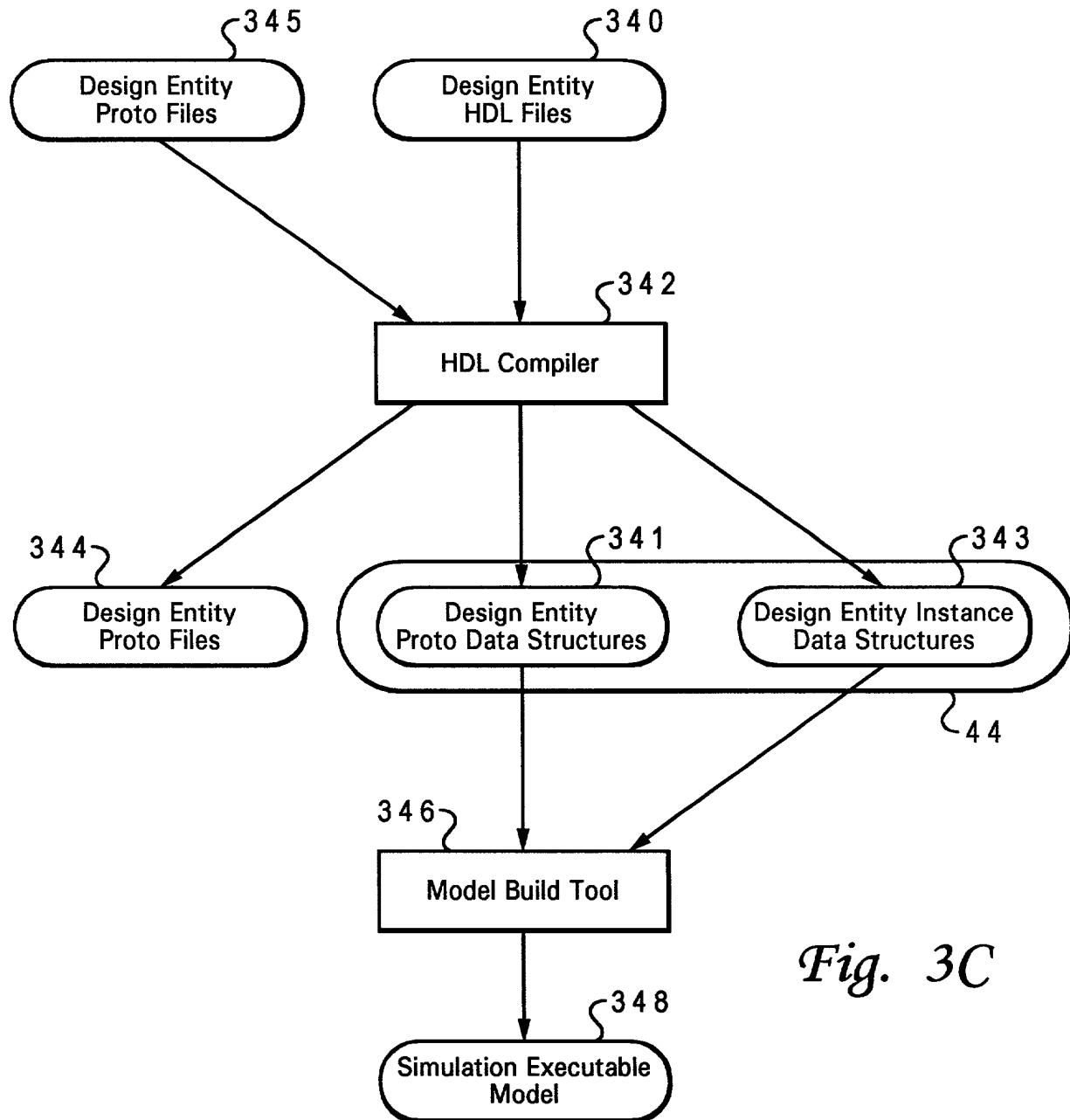


Fig. 3C

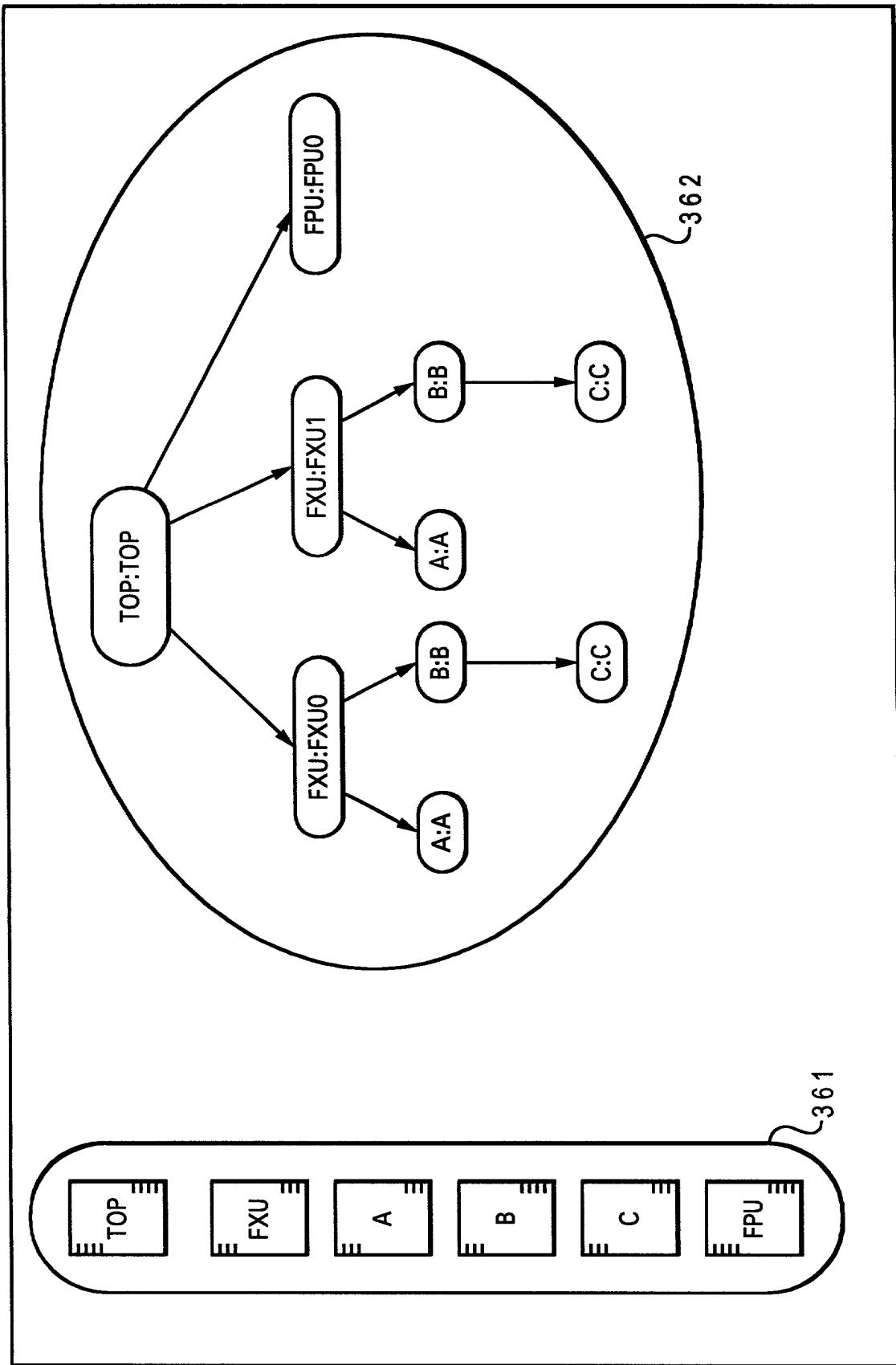


Fig. 3D

44

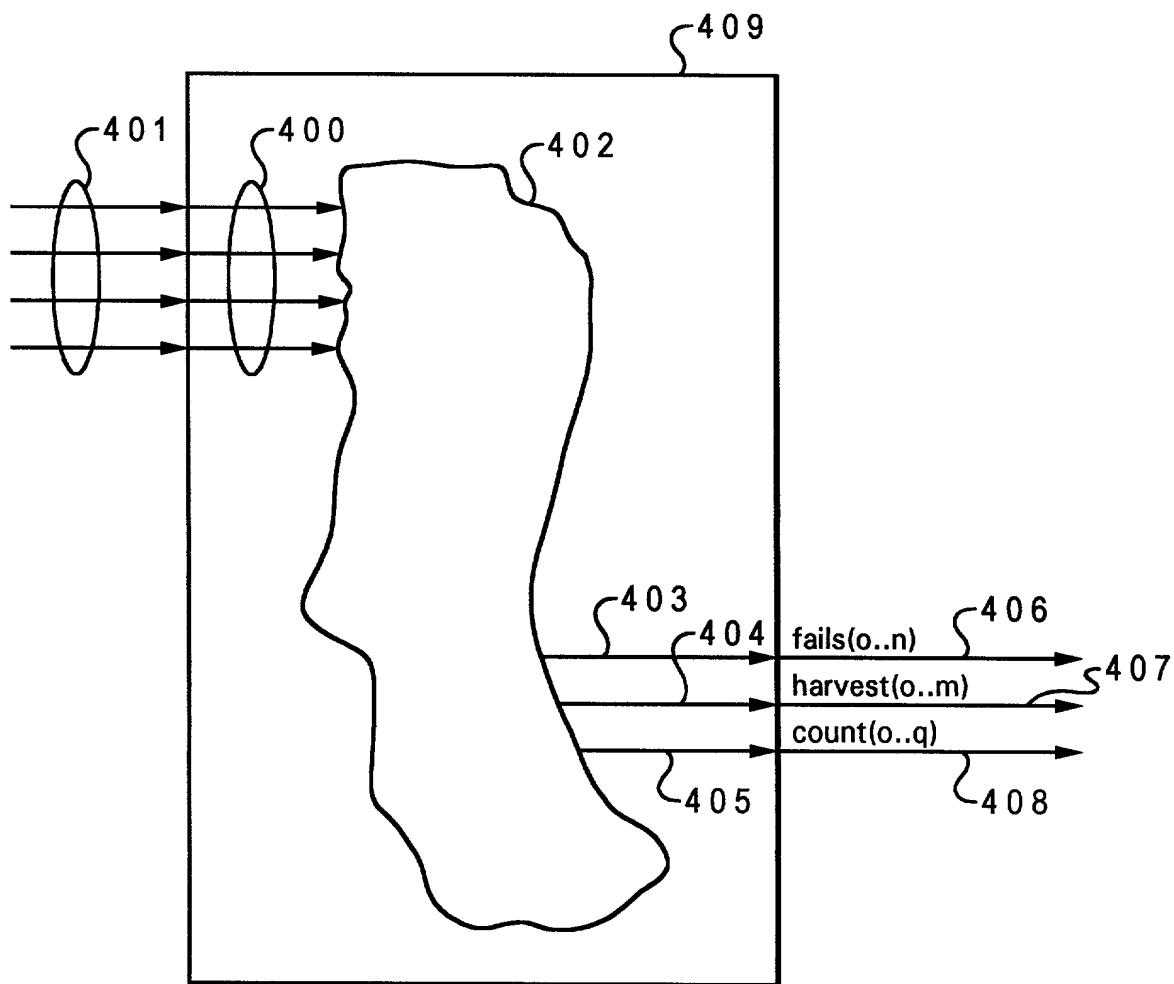


Fig. 4A

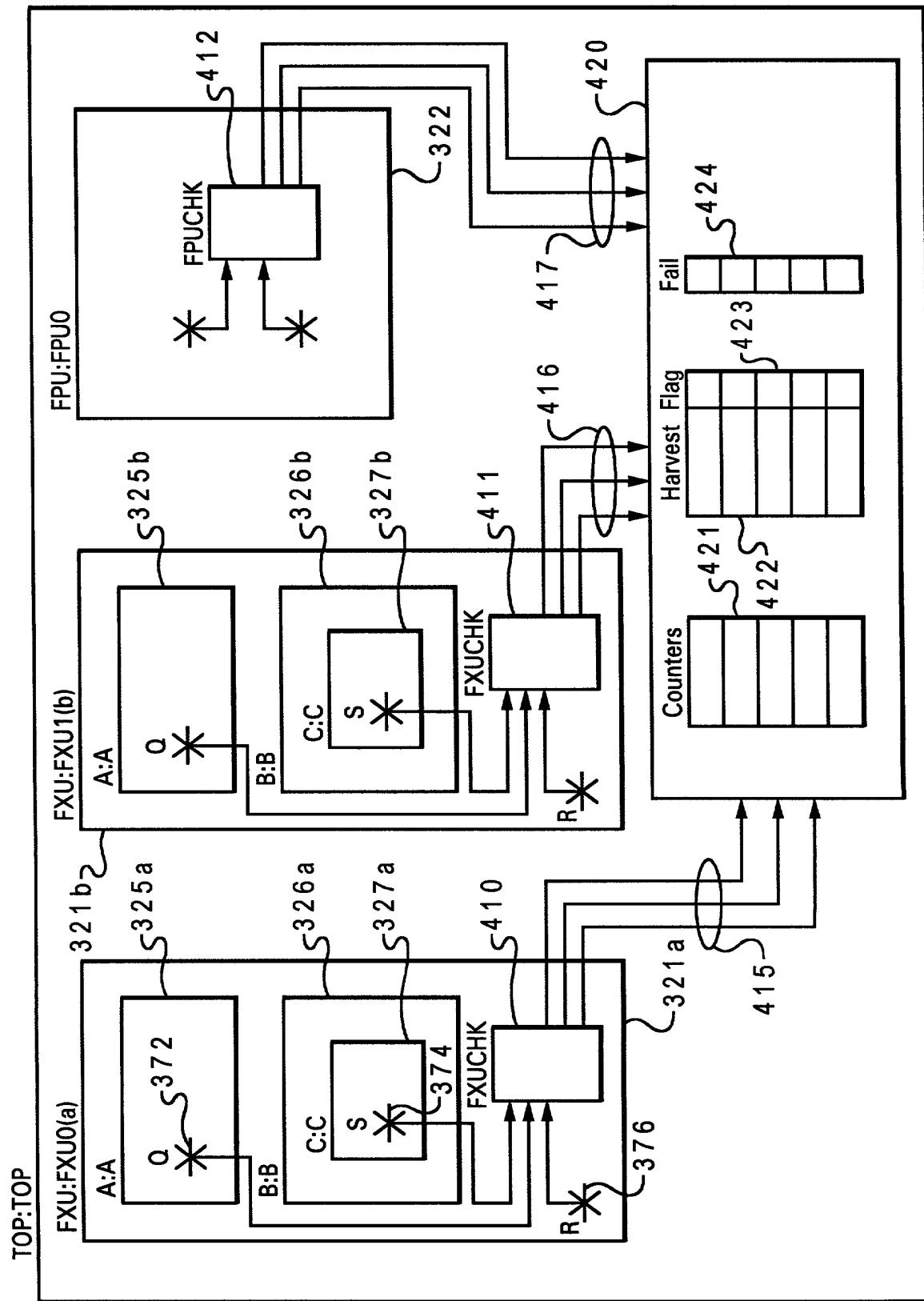


Fig. 4B

329

```

ENTITY FXUCHK IS
  PORT(  S_IN      : IN std_ulogic;
          Q_IN      : IN std_ulogic;
          R_IN      : IN std_ulogic;
          clock     : IN std_ulogic;
          fails     : OUT std_ulogic_vector(0 to 1);
          counts    : OUT std_ulogic_vector(0 to 2);
          harvests  : OUT std_ulogic_vector(0 to 1);
);

```

450

452 {
--!! BEGIN
--!! Design Entity: FXU;

453 {
--!! Inputs
--!! S_IN => B.C.S;
--!! Q_IN => A.Q;
--!! R_IN => R;
--!! CLOCK => clock;
--!! End Inputs

454 {
--!! Fail Outputs;
--!! 0 : "Fail message for failure event 0";
--!! 1 : "Fail message for failure event 1";
--!! End Fail Outputs;

455 {
--!! Count Outputs;
--!! 0 : <event0> clock;
--!! 1 : <event1> clock;
--!! 2 : <event2> clock;
--!! End Count Outputs;

456 {
--!! Harvest Outputs;
--!! 0 : "Message for harvest event 0";
--!! 1 : "Message for harvest event 1";
--!! End Harvest Outputs;

457 {
--!! End;

440

451

458 {
ARCHITECTURE example of FXUCHK IS
BEGIN
... HDL code for entity body section ...
END;

Fig. 4C

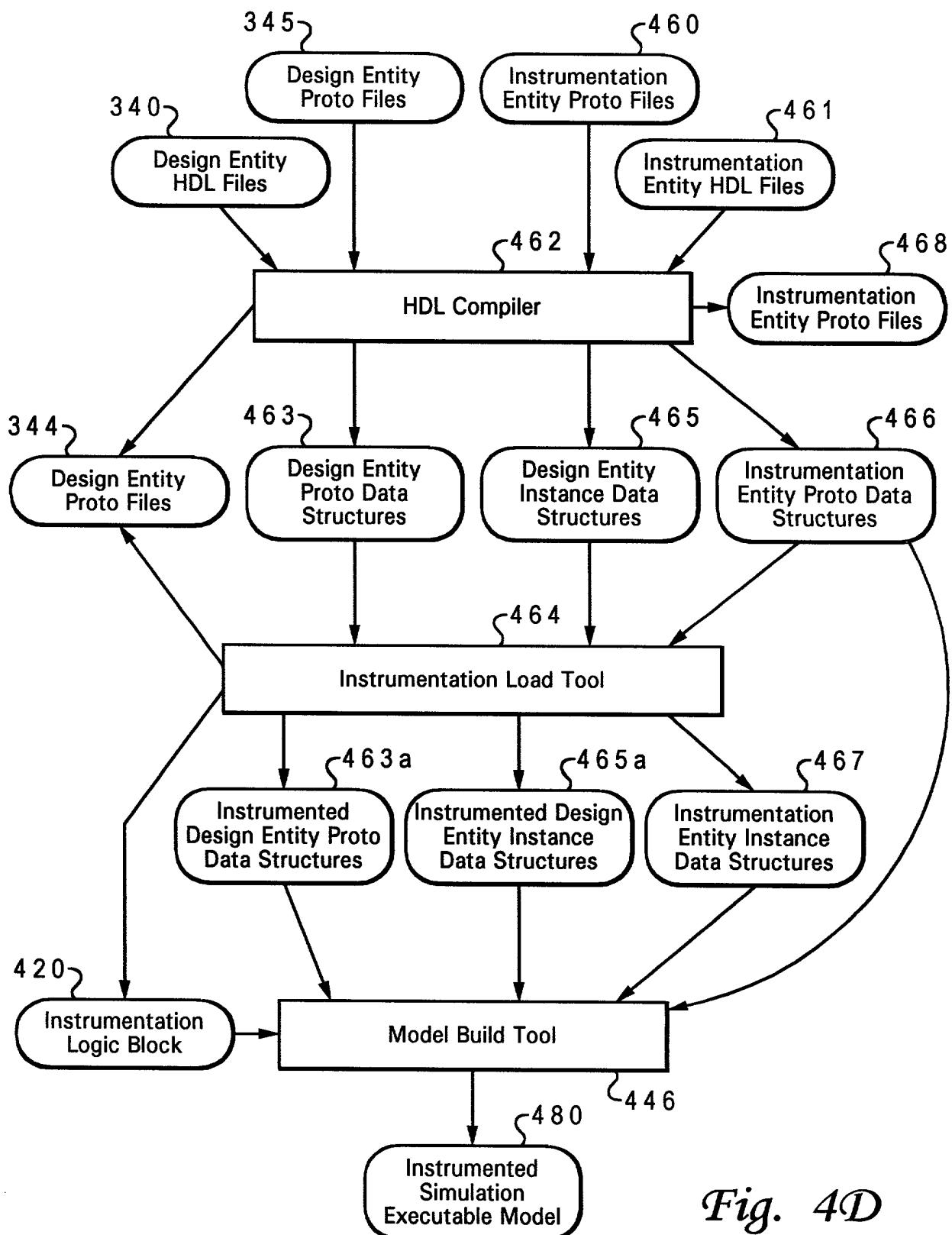


Fig. 4D

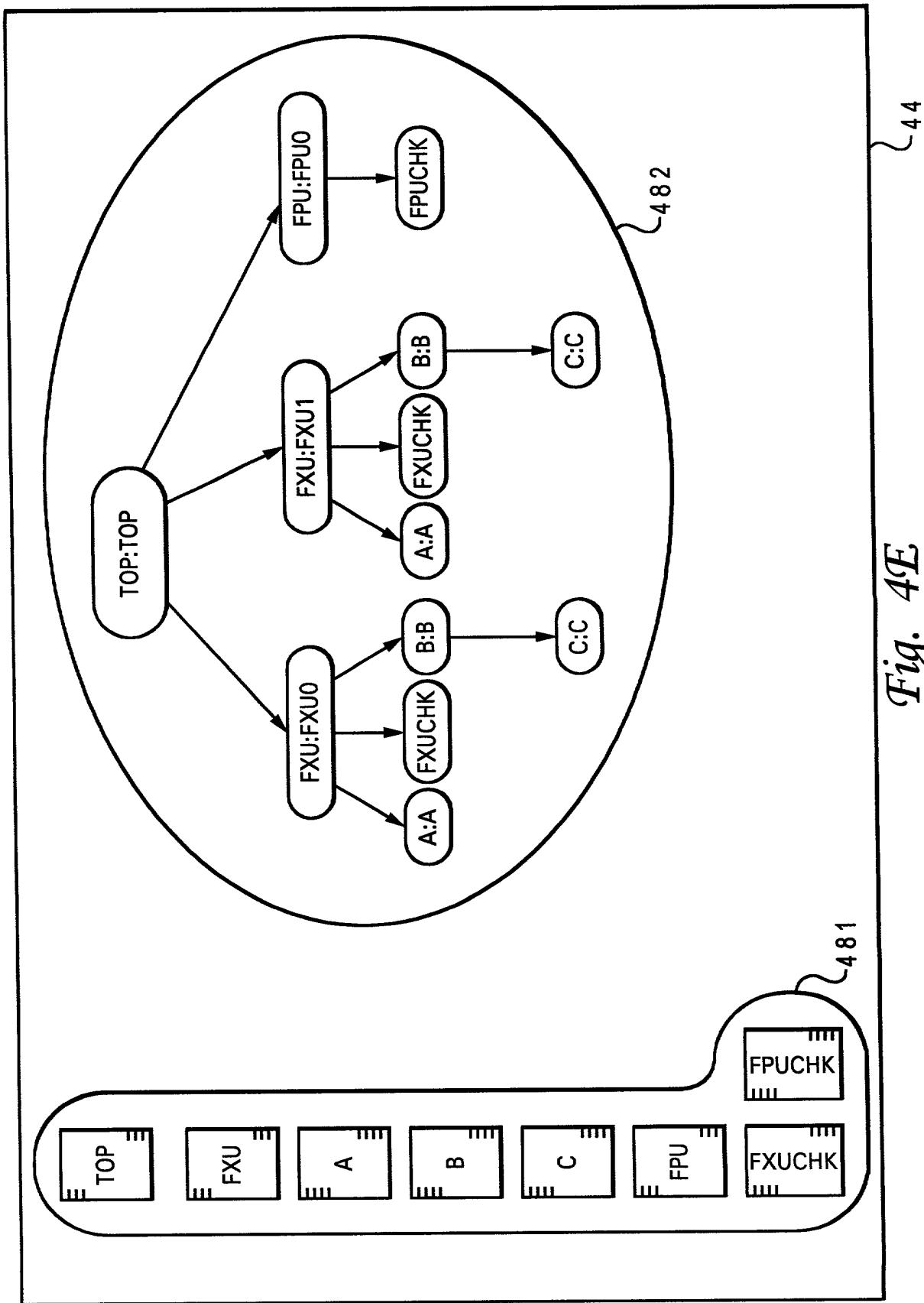


Fig. 4E

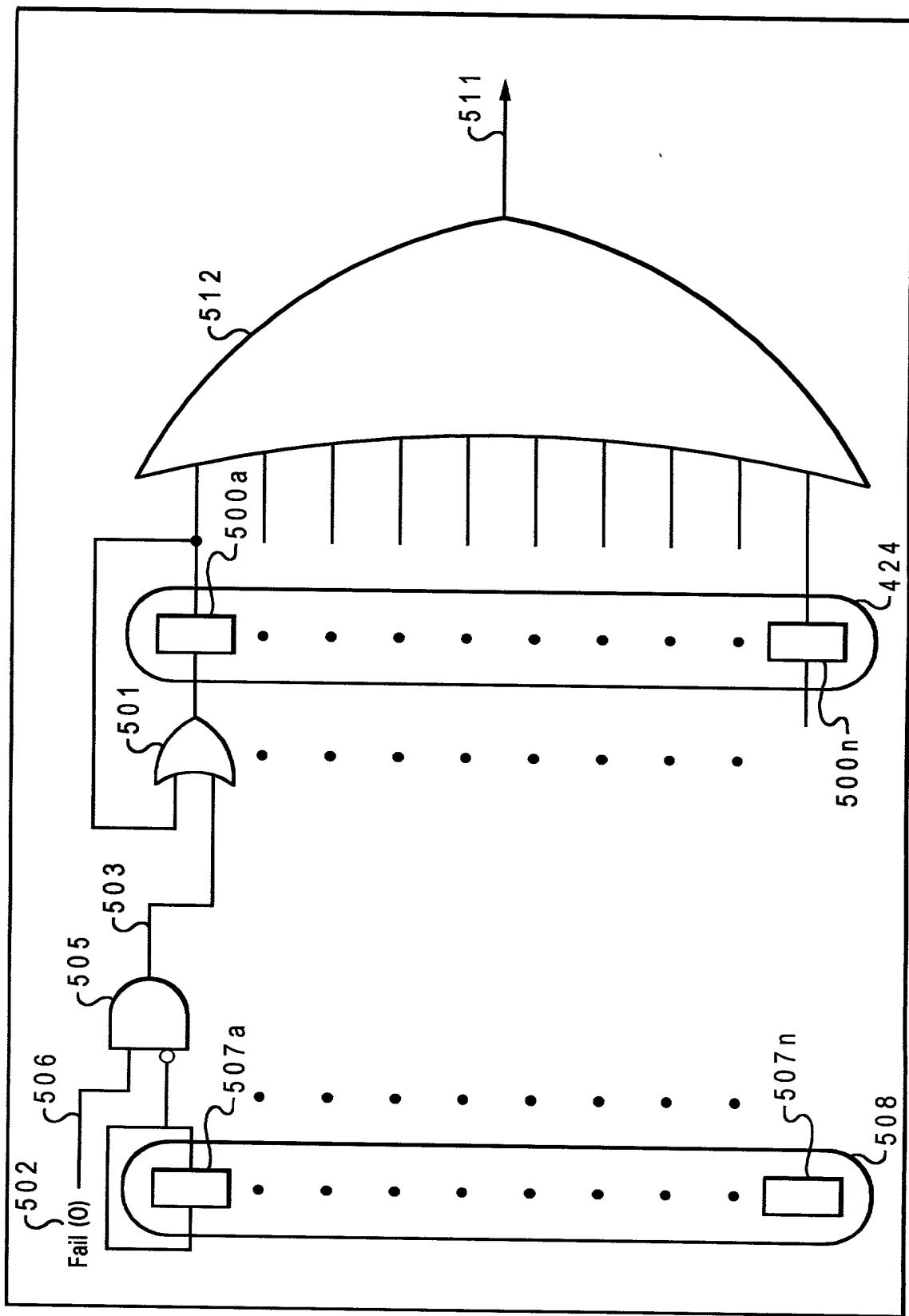


Fig. 5A
420

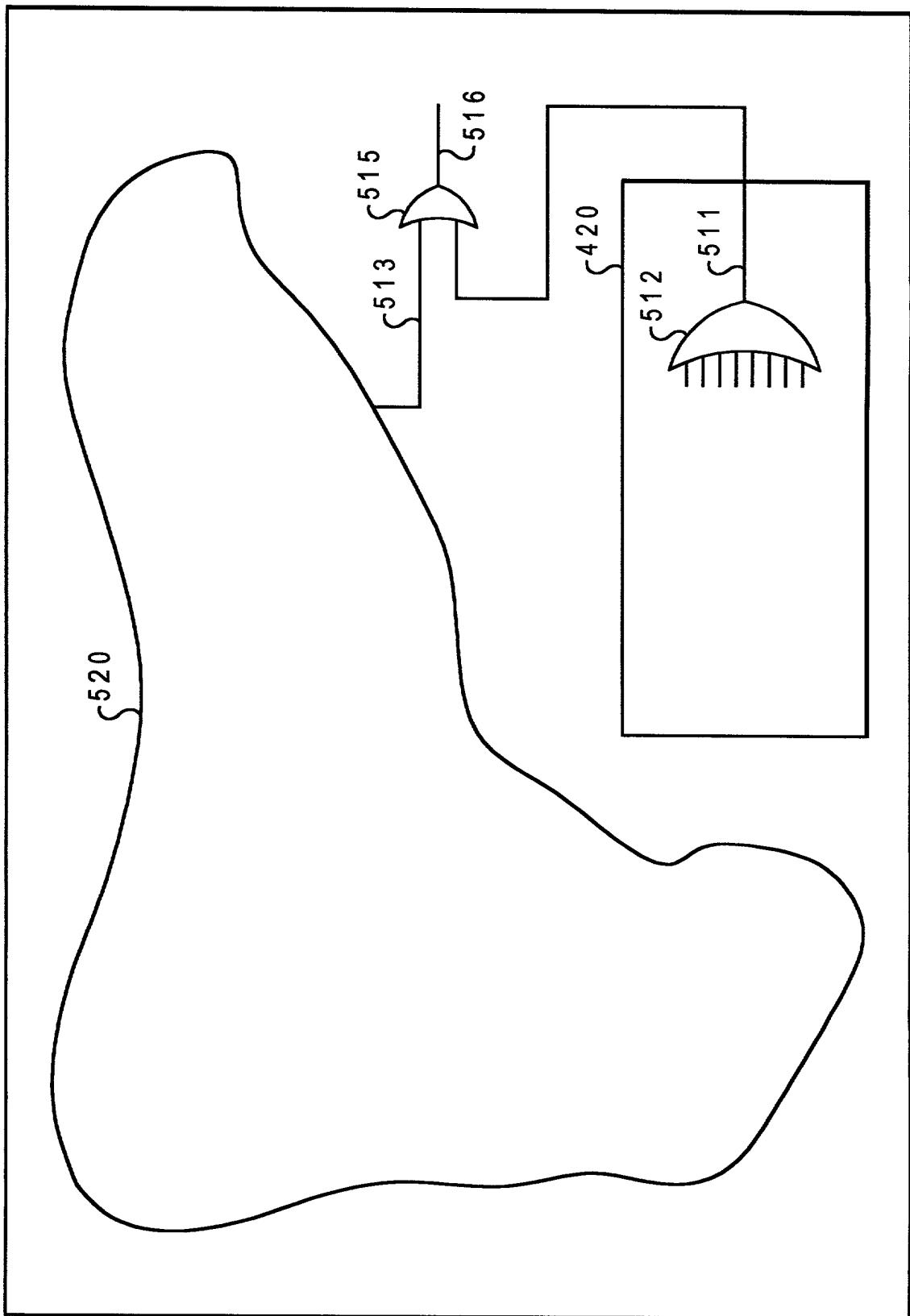


Fig. 5B

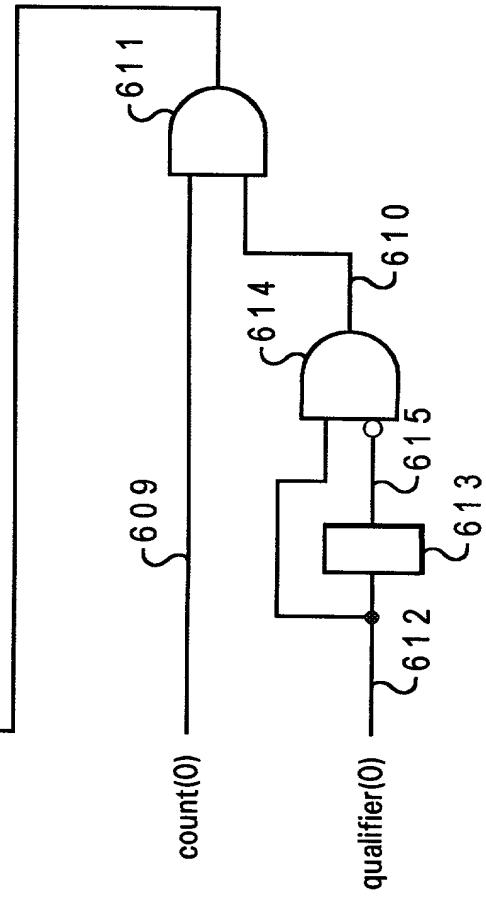
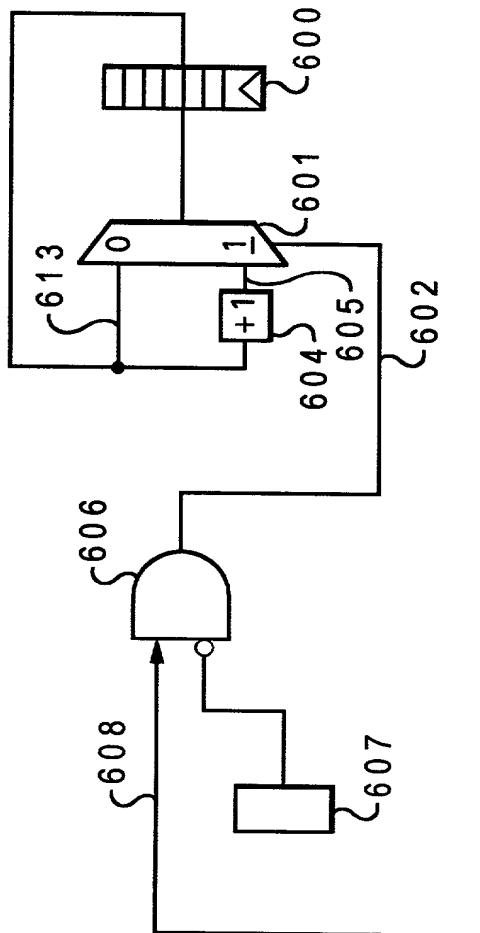


Fig. 6A

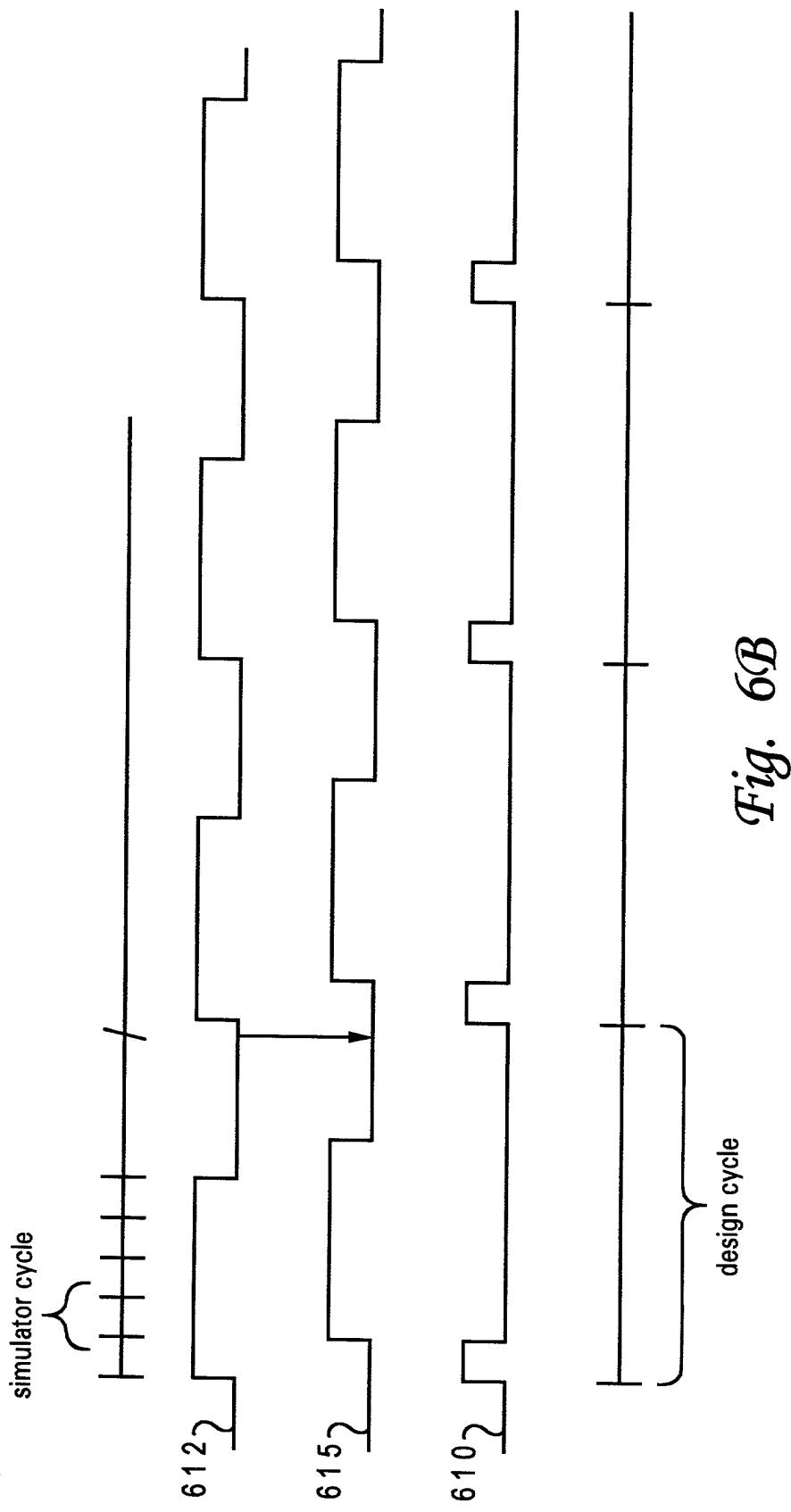


Fig. 6B

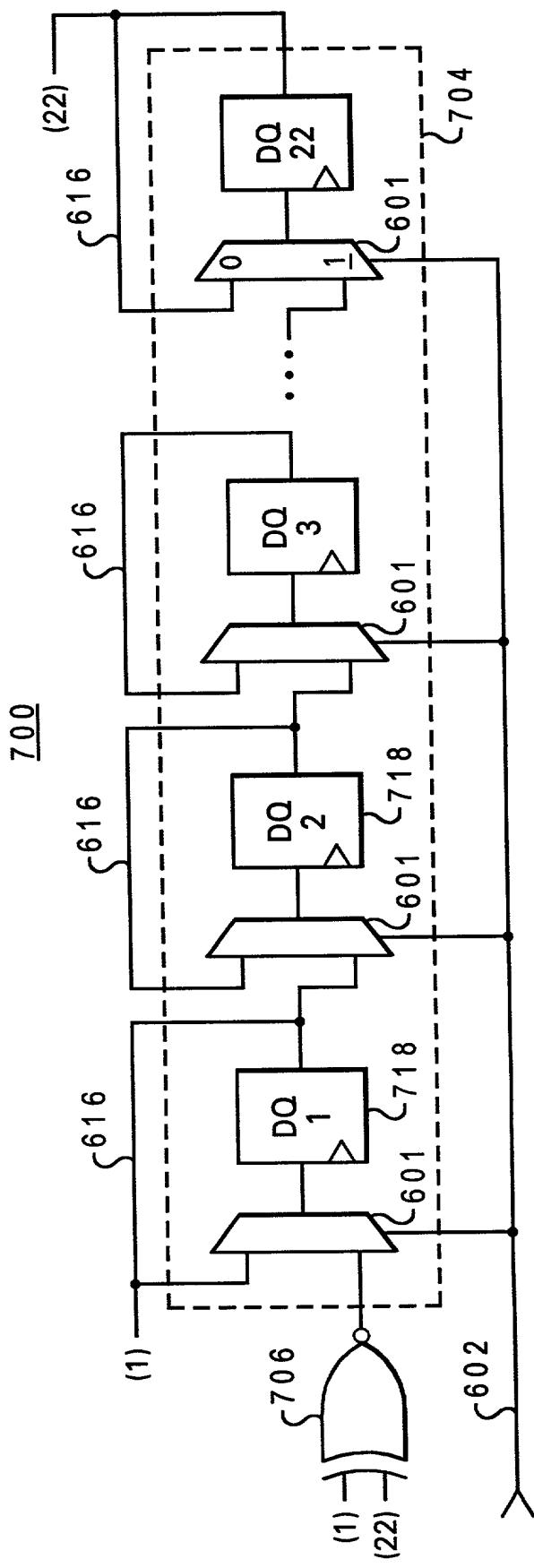


Fig. 7

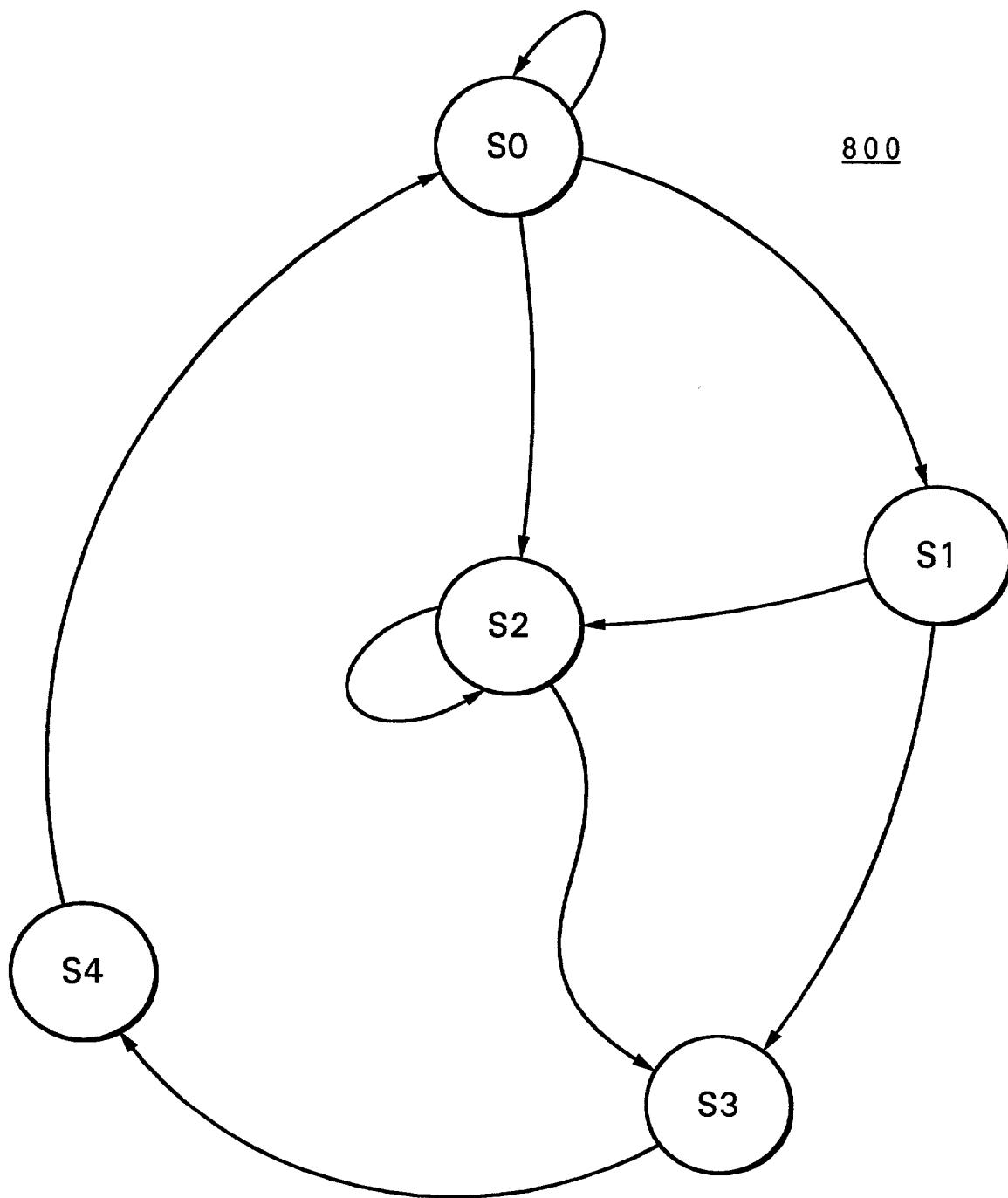


Fig. 8A
Prior Art

entity FSM : FSM

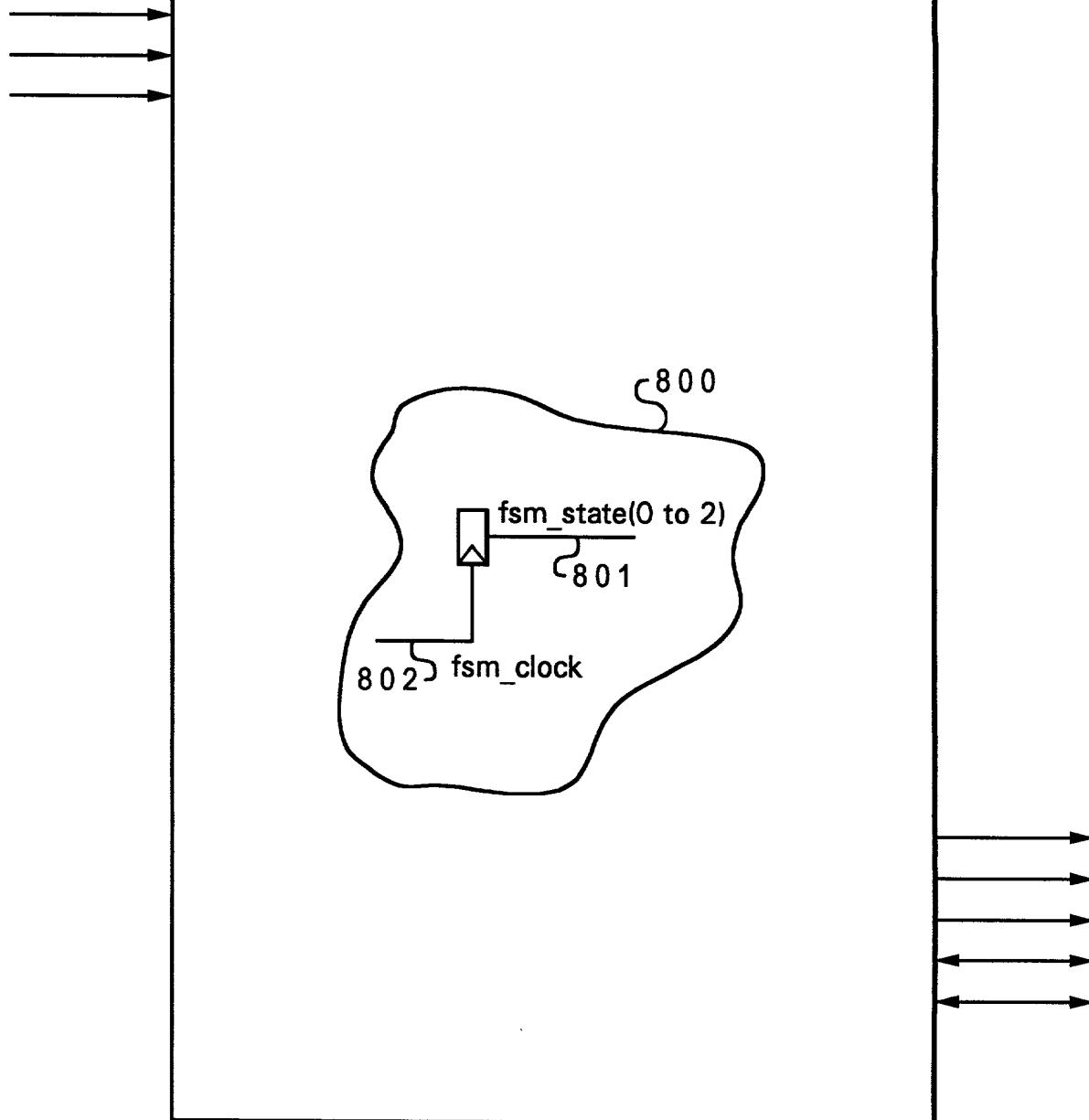
850

Fig. 8B
Prior Art

ENTITY FSM IS

```
PORT(
    ....ports for entity fsm....
);
```

ARCHITECTURE FSM OF FSM IS

BEGIN

... HDL code for FSM and rest of the entity ...

fsm_state(0 to 2) <= ... Signal 801 ...

```
853 { --!! Embedded FSM : example fsm;
859 { ---!! clock          : (fsm_clock);
854 { ---!! state_vector   : (fsm_state(0 to 2));
855 { ---!! states         : (S0, S1, S2, S3, S4);
856 { ---!! state_encoding : ('000', '001', '010', '011', '100');
857 { ---!! arcs           : (S0 => S0, S0 => S1, S0 => S2,
858 { ---!!                   (S1 => S2, S1 => S3, S2 => S2,
                                (S2 => S3, S3 => S4, S4 => S0); }
```

END;

Fig. 8C

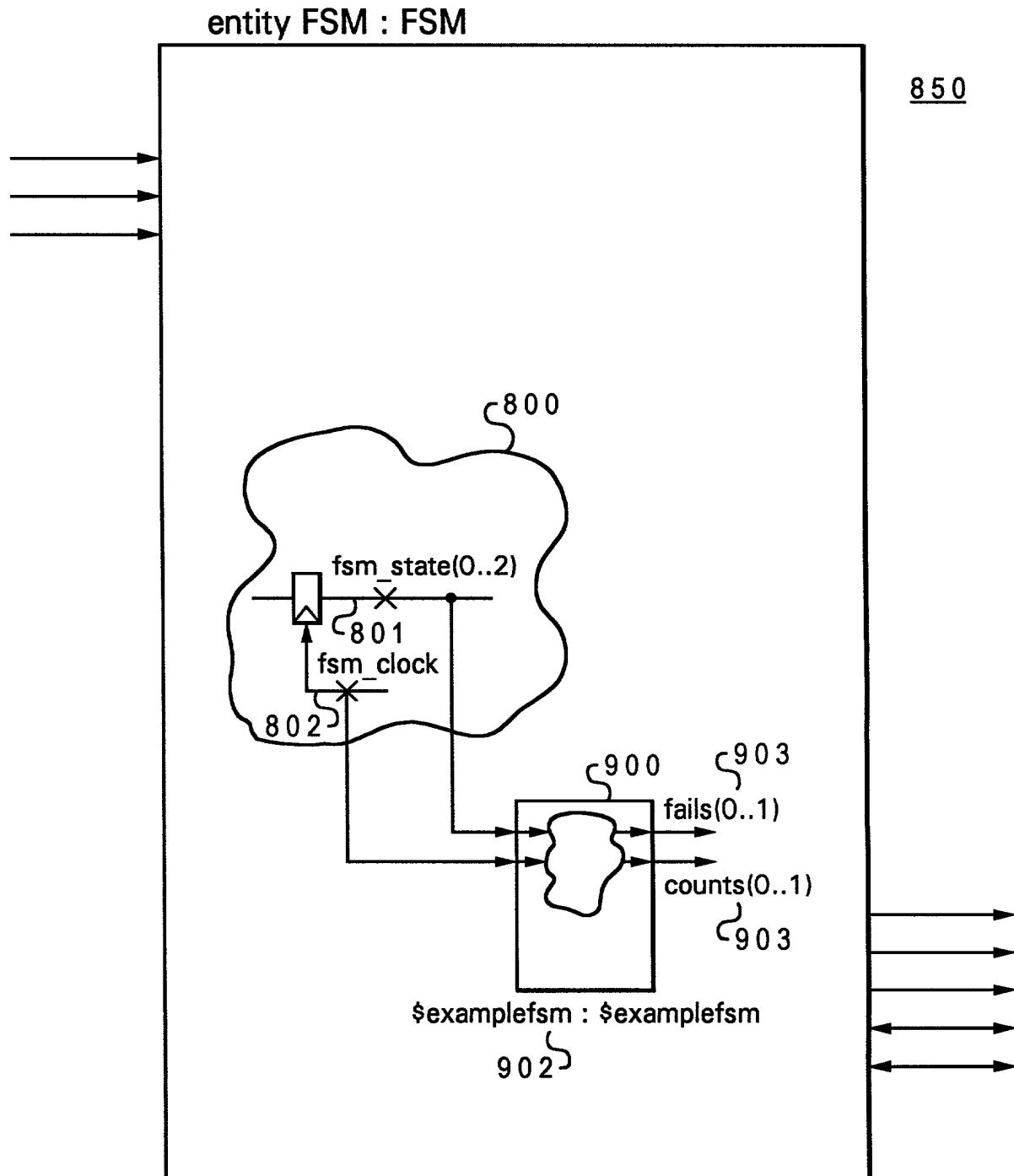
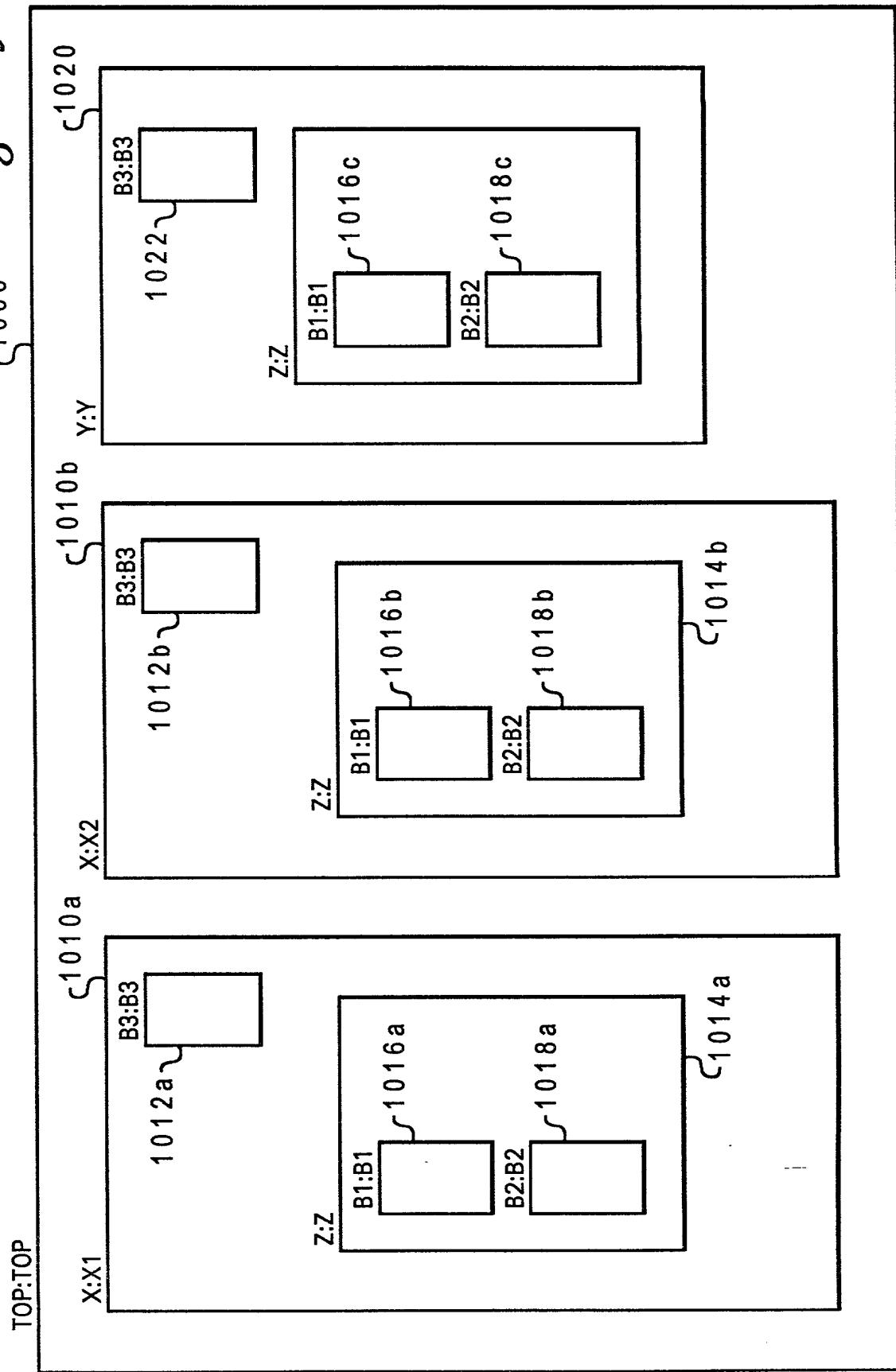


Fig. 9

Fig. 10A



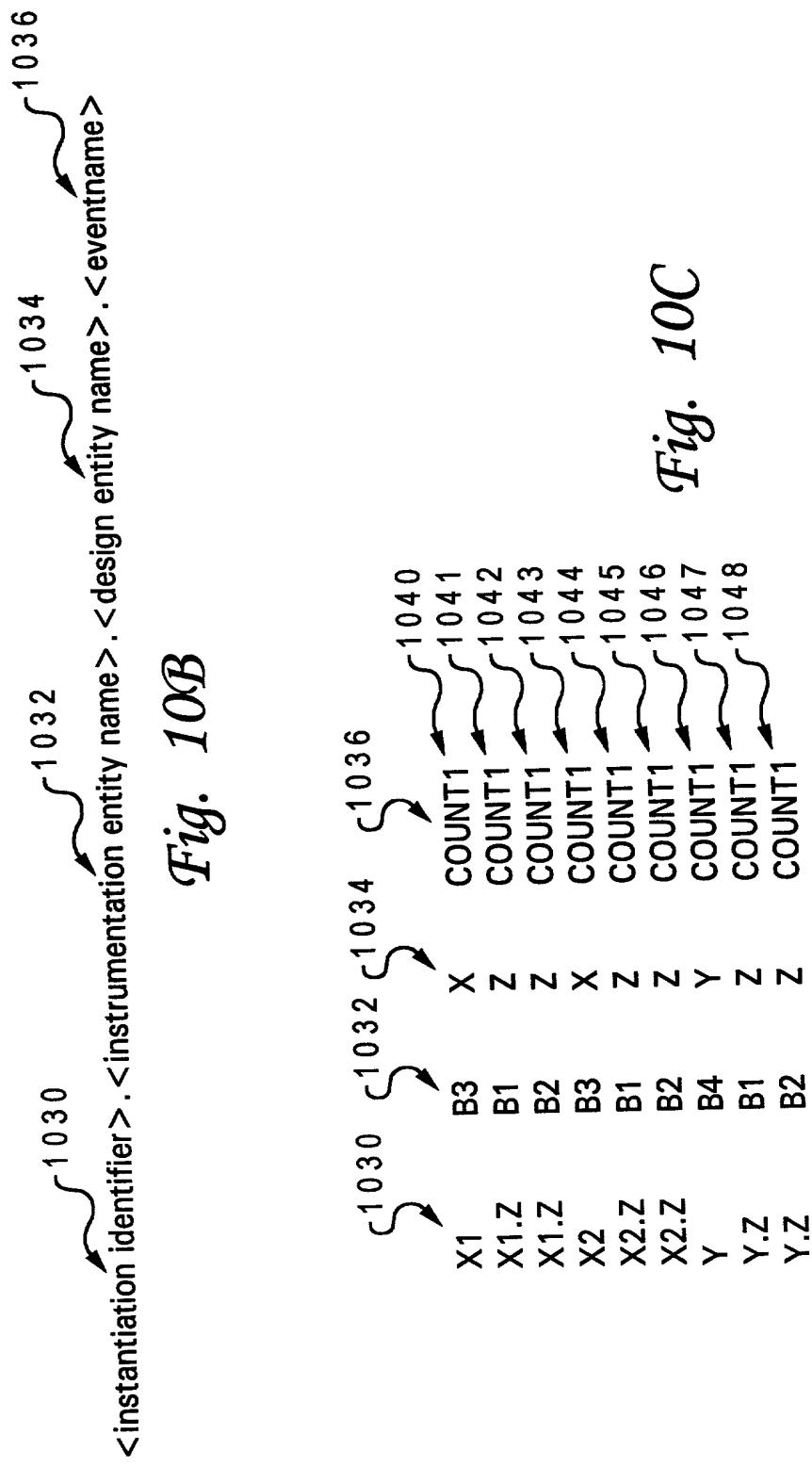


Fig. 10B

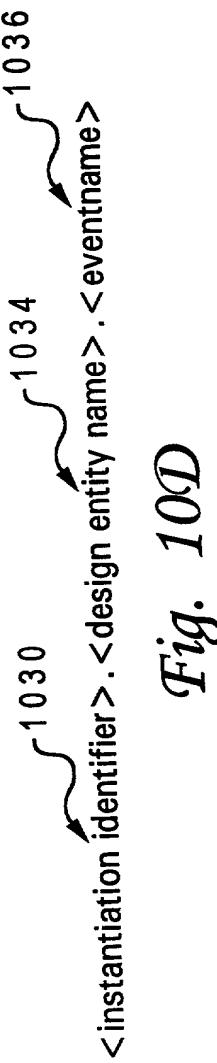
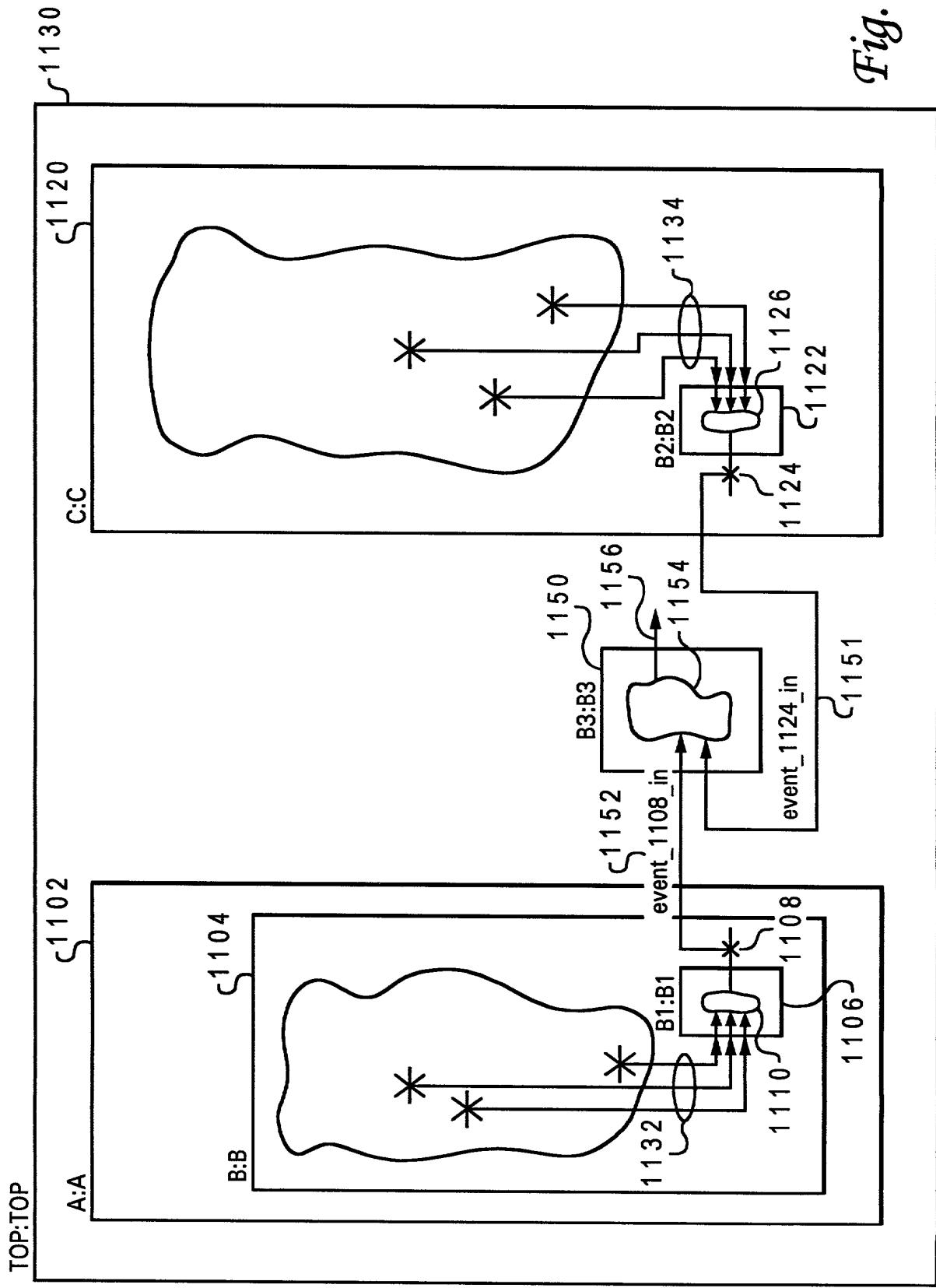


Fig. 11A



--!! Inputs
--!! event_1108_in <= C.[B2.count.event_1108]; ~1161
--!! event_1124_in <= A.B.[B1.count.event_1124]; ~1162
--!! End Inputs

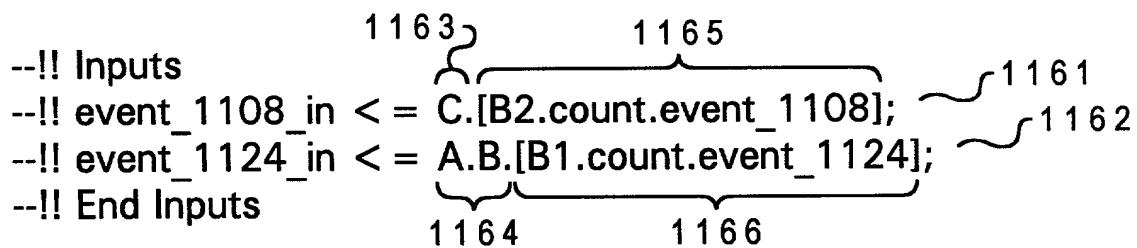


Fig. 11B

--!! Inputs
--!! event_1108_in <= C.[count.event_1108]; ~1171
--!! event_1124_in <= B.[count.event_1124]; ~1172
--!! End Inputs

Fig. 11C

Fig. 12A

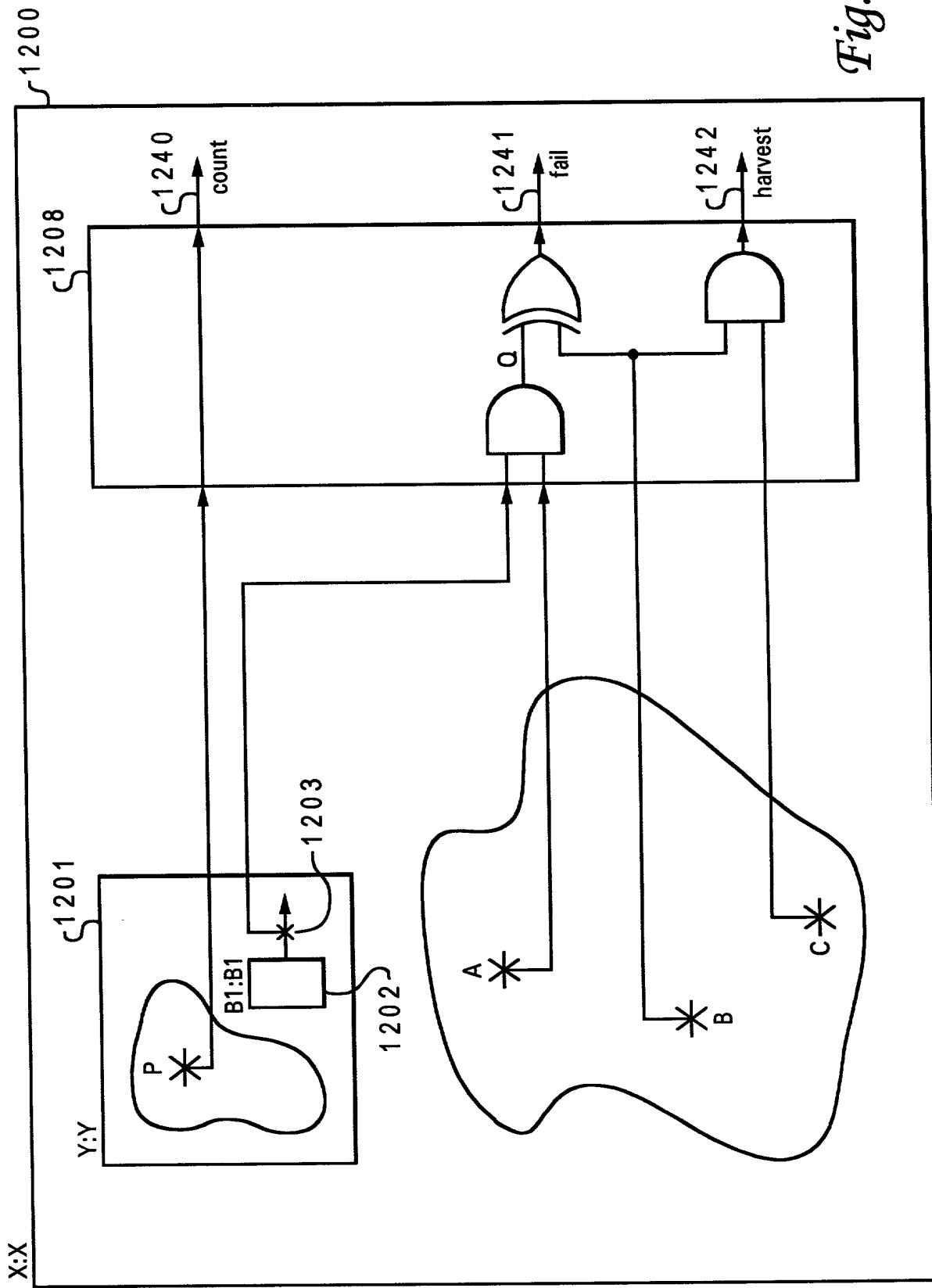


Fig. 12B